College of Engineering and Computer Science
CMPE 4375 / ELEE 4375 – Introduction to VLSI Design
Syllabus Spring 2019

Course Name: Introduction to VLSI Design
Course Number: CMPE 4375 / ELEE 4375

PREREQUISITE: Prerequisites: CMPE/ELEE 2330 and ELEE3301/CMPE 3403.
with a grade of ‘C’ or better. Students are expected to be familiar with digital logic gates; NAND, NOT, NOR gates, and MOSFET properties.
All Electrical Engineering and Computer Engineering as well as Computer Science students are eligible to take this course as elective

Instructor: Dr. Nazmul Islam, Electrical Engineering,
Office: ENGR 3.277;
Office phone: 665-7228
Nazmul.Islam@utrgv.edu

CLASS TIMES: T R 3:05pm – 4:20pm EIAB 2.205 (New Intedisc Engin &Acad Bldg, Edingurg)

Office Hour: M T W R : 2:00pm – 3:00pm.

IT Help: Mr. Robert Jackson; robert.jackson@utrgv.edu [for Log in problem]

Objectives To introduce the study of VLSI DESIGN, with emphasis on CMOS VLSI, and Integrated Circuit (IC) design using CAD Tools: CADENCE (for Schematic, Layout, Simulation)

- Physical operation of different logic gates
- Continuation of CMOS technology
- Introduction to Very Large Signal Integration (VLSI) design
- Digital circuits design concepts such as Flip Flops, Counters
- Layout of Inverter, NAND, NOT, NOR, XOR gates using metal oxide semiconductor field-effect transistors (MOSFETs), NMOS, PMOS
- Schematic, Layout and simulation of different digital circuit
This will be a **project-based course**, where students will do **Cadence** simulation and layout for final project and **send the design to MOSIS for micro-fabrication**.

**Text**
CMOS Digital Integrated Circuits Analysis & Design *4th Edition*
by Sung-Mo (Steve) Kang, Yusuf Leblebici, Chul Woo Kim; 2014;

**Reference**
Class handouts
- Cadence manual set
- H.Craig Casey, Jr., *Devices for Integrated Circuits*, John-Wiley,

**Grade**
- 20% homework and Quizzes
- 20% mid-term exam
- 15% final exam
- 45% Labs and projects
  
  **Laboratory Based Projects**
  Final project include design, report and presentation

**Project, Homework, and Exam:**
Homework and Projects must be turned in when due; late homework and projects are not encouraged. Although makeups are discouraged, it is possible to makeup a major exam due to sickness, but only one makeup is allowed per semester.

**Grading Scale**
A(>90%), B(89-80%), C(79-70%), D(60 - 69%), F(<60%)

**Note:**
To pass the course, a student must complete all labs and design projects. The Final project may be carried out by a team of 2 students.

**Class**

<table>
<thead>
<tr>
<th>Topic</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Week 1</strong></td>
</tr>
<tr>
<td>Introduction to NMOS, PMOS, CMOS logic gates</td>
</tr>
<tr>
<td><strong>Week 1/2</strong></td>
</tr>
<tr>
<td>Transfer curve, Noise margin, Gate delays, Rise time, Fall time, Introduction to CAD simulation.</td>
</tr>
</tbody>
</table>
Week 2/3
CMOS Processing, Schematic, Layout, simulation and related issues; Integrated circuit (IC) design

Week 3
Pseudo NMOS logic; Pseudo NMOS logic gates; CMOS logic, CMOS gate design;

*Midterm*

Week 4
Transmission gates; Fully differential CMOS Logic;

Week 4/5
Latches, Flip Flops; Synchronous system design

Week 5
Final Project assigned
Digital Integrated System Building Blocks

**Final Examination: on Cadence Design**

**Outcomes** (department student learning outcomes)
(A1) knowledge of differential and integral calculus;
(A2) knowledge of probability and statistics;
(A4) knowledge of transform techniques;
(A5) knowledge of basic linear algebra and discrete mathematics;
(A6) an ability to apply the above techniques to engineering problems.

(E1) knowledge of at least one specialization area within electrical engineering that goes beyond the basic skills expected of all electrical engineering students.

(F1) successful completion of multiple design projects that incorporate material from more than one course or technical area, including open-ended projects that have a variety of possible solutions.

**At the end of the semester, it is expected that students should be able to:**
(1) To understand CMOS Technology
(2) To design layout and schematic and analysis digital logic gates
(3) To simulate different logic gates using industry standard software CAD tools Cadence
(4) To explain the purpose and applications of CMOS technology
(5) To be familiar with Digital Integrated Circuits and System Building Blocks

**ADA Notice:** If you have any disability which will make it difficult for you to carry out the work as I have outlined and/or if you need special accommodations/assistance due to a disability please contact the Office of Services for Persons with Disabilities, Emilia Hall Room 100 immediately. Appropriate arrangements/accommodations can be arranged.